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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/665,993
Filing Date: September 18, 2003
Appellant(s): SINGH ET AL.

International Business Machines Corporation
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/7/06 appealing from the Office action mailed 1/30/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The amendment after final rejection filed on 3/30/06 has not been entered.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

20040222859	Hajimiri et al.	11-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-4, 7, & 8 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Application No. 2004/0222859 Hajimiri et al.

1. Referring to claim 1, a vertically stacked coplanar transmission line structure for an integrated circuit (IC) chip defining a closed ground return path, (Paragraph 0028, where the Lines #602, 604, & 606 are signal lines and in order for a signal to flow through a conductor there must be a potential applied to the ends of the conductor and where a circuit must be a closed circuit in order to operate), within the transmission line structure, comprising: a micro-strip pair of first, (Figure 5B #600A), and second vertically stacked coplanar conductors, (Figure 5B #600A), each first and second vertical stack comprising a metal layer, (Figure 5A #606), a next metal layer down, (Figure 5A #602), and an intermediate connecting via layer, (Figure 5A #604), in between the metal layer, (Figure 5A #606), and the next metal layer down, (Figure 5A #602), said intermediate connecting via layer, (Figure 5A #604), comprising a via bar, (Figure 5A #604), having a width dimension approximately equal to a width dimension of said first and second vertically stacked coplanar conductors, (Figure 5A #602 & 606), and having a length dimension approximately equal to a length dimension of said first and second vertically stacked coplanar conductors, (Figure 5A #602 & 606).

2. Referring to claim 2, a transmission line structure, wherein each vertically stacked coplanar conductor comprises metal in the metal layer m(i), (Figure 5A #606), metal in the next metal layer down m(i-1), (Figure 5A #602), and metal in the intermediate connecting via layer, (Figure 5A #604).

3. Referring to claim 3, a transmission line structure, fabricated in upper metal layers of the IC chip, (lower metal layer #24b).

4. Referring to claim 4, a transmission line structure, wherein the intermediate connecting via layer comprises a single via bar, (Figure 5A #604), which extends across an entire width of the intermediate connecting via layer, (Figure 5A #604).

7. Referring to claim 7, a transmission line structure, wherein the micro-strip pair of first and second vertically stacked coplanar conductors comprise a differential positive and negative pair of transmission line conductors, (Paragraph 0028, where the Lines #602, 604, & 606 are signal lines and in order for a signal to flow through a conductor there must be a potential applied to the ends of the conductor).

8. Referring to claim 8, a transmission line structure, wherein the micro-strip pair of first and second vertically stacked coplanar conductors comprise signal and ground transmission line conductors, (Paragraph 0028, where the Lines #602, 604, & 606 are signal lines and in order for a signal to flow through a conductor there must be a potential applied to the ends of the conductor).

(10) Response to Argument

A. The Applicant argues that U.S. Patent Application Publication No. 2004/0222859 Hajimiri et al. does not teach the transmission lines to be formed as a microstrip structure. The Applicant continues to argue that Hajimiri et al. teaches of a traveling wave amplifier structure or TWAS as shown in Hajimiri et al. Figure 2, which can be found on page 6 lines 10-13 of the Appeal Brief. The examiner disagrees with the Applicant's arguments because Hajimiri et al. teaches in paragraph 0016 lines 3-11 that the TWAS structure's transmission lines can be implemented as a micro strip line. It is clear that the Hajimiri et al. structure does teach the transmission lines to be formed as a microstrip structure.

B. The Applicant argues that Hajimiri et al. does not teach the transmission line structure to be formed in a stack configuration. The examiner disagrees with the Applicant's arguments because in Hajimiri et al.'s Figure 5A, (see below), it is clear that the transmission lines labelled #602 and 606 are vertically stacked and separated by an unspecified distance.

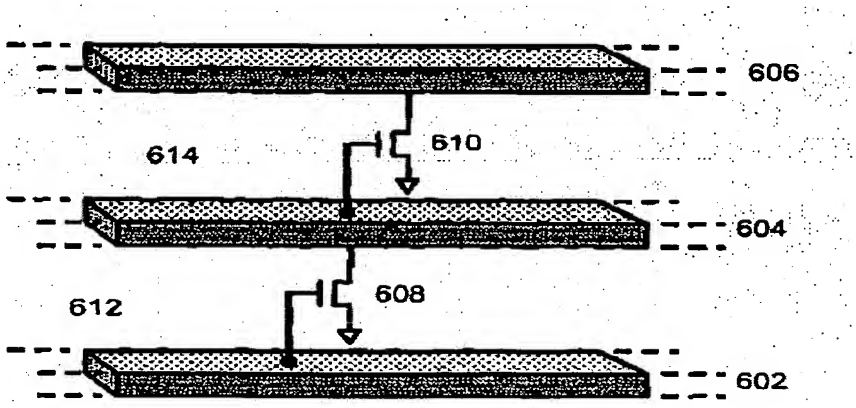
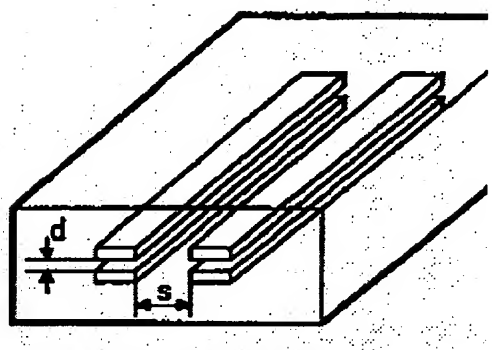


FIGURE 5A 600A

U.S. Patent No. 6,961,229 Osuka et al. Figure 5C, (see below and used as a teaching reference), also teaches transmission lines being vertically stacked and separated by an unspecified distance labelled by (d).

FIG.5C



stacked pair lines

Hajimiri et al. and Osuka et al. by evidence of the figures shown above teaches a common definition for stacked transmission lines, hence it is commonly known in the art that Hajimiri et al. does teach the claimed limitation of claim 1 of a vertically stacked transmission line.

The Applicant also argues that Hajimiri et al. does not teach a pair of coplanar vertically stacked transmission lines. The examiner disagrees because in Hajimiri et al. Figure 5B, (see on the next page), teaches a first set of vertically stacked transmission lines, (examiner's label #1), and a second set of vertically stacked transmission lines, (examiner's label #2), being vertically coplanar. Hajimiri et al. Figure 5B also teaches #600A to be the structure of Hajimiri et al. Figure 5A #600A. The evidence detailed in Hajimiri et al. Figure 5 A&B teaches a pair of coplanar vertically stacked transmission lines as recited in claim 1.

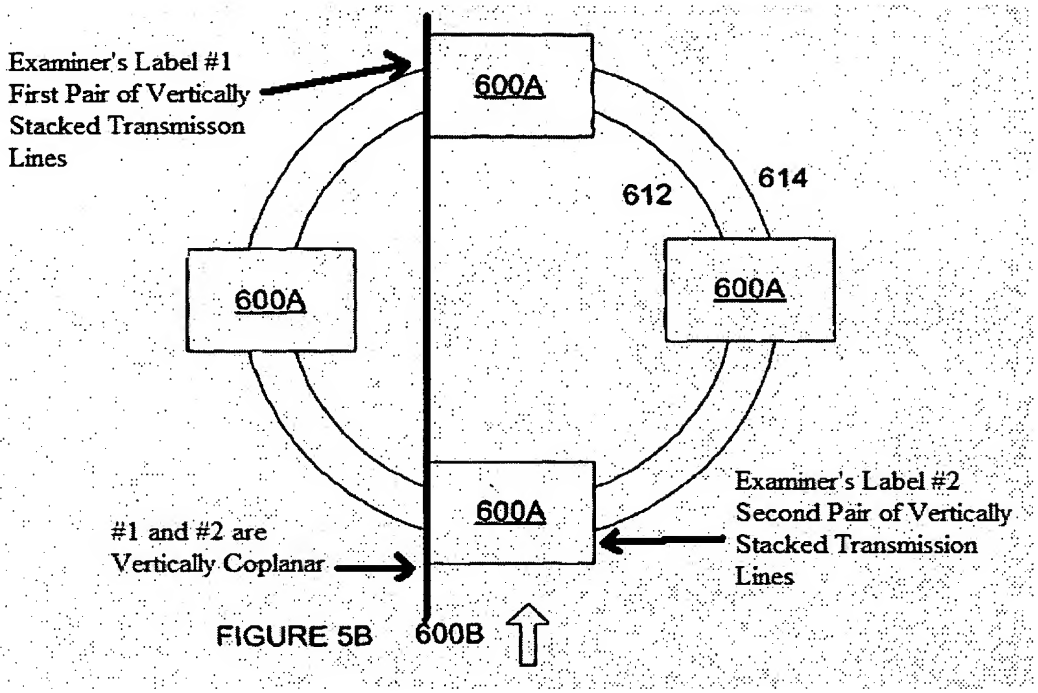


FIGURE 5B

C. The Applicant argues that Hajimiri et al. does not teach a conductive via bar layer in intermediate connection with the top metal layer and the underlying metal layer in each vertically stacked structure. The examiner disagrees with the Applicant because although the Applicant uses terms different to those of Hajimiri et al. to label the claimed invention, this does not result in any structural difference between the claimed invention and the prior art. Note that the use of different terminology to describe the via bar layer in intermediate connection with the top metal layer and the underlying metal layer in each vertically stacked structure is just a writing style and the way in which a structural limitation is expressed does not affect the configuration of the described elements. Hajimiri et al. in Figure 5A, (see above), teaches a conductive layer in the shape of a bar, (Hajimiri et al. in Figure 5A #604), that is positioned between and intermediately connected with the top metal layer, (Hajimiri et al. in Figure 5A #606), and the underlying metal layer, (Hajimiri et al. in Figure 5A #602), in each vertically stacked structure. The term intermediate connection is read as a functional limitation where the

via bar layer, (Hajimiri et al. in Figure 5A #604), is electrically connected to the top metal layer, (Hajimiri et al. in Figure 5A #606), and the bottom metal layer, (Hajimiri et al. in Figure 5A #602), via transistors, (Hajimiri et al. in Figure 5A #608 and 610).

D. The Applicant argues that Hajimiri et al. does not teach the transmission lines to have equal length and width. The examiner disagrees because in Hajimiri et al. Figure 6A, (see below), teaches of a similar transmission line structure where the transmission lines are illustrated to have different widths and lengths, which can be seen by comparing transmission line #706 with transmission line #704. Hajimiri et al. Figure 5A, (see above), teaches and illustrates the transmissions #602 and 606 to have the same width and length.

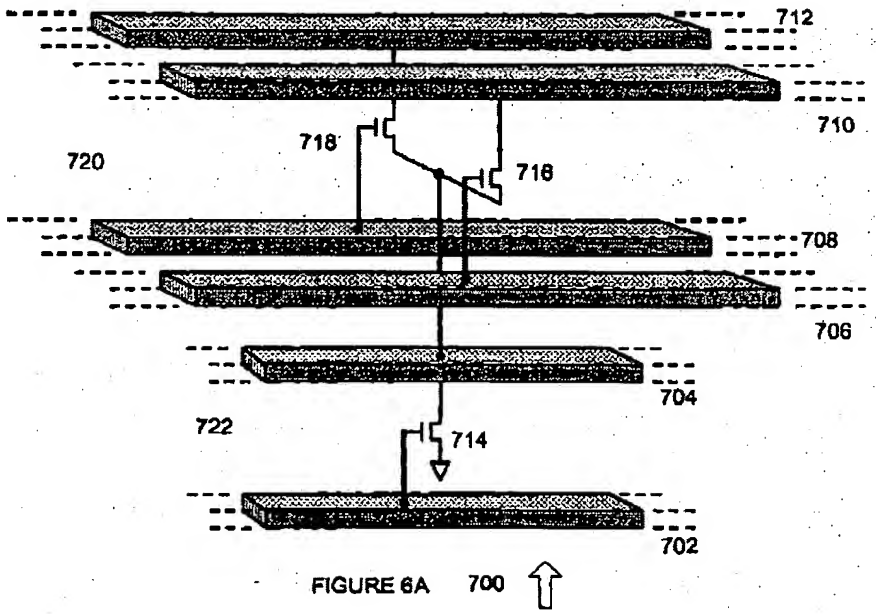


FIGURE 6A 700

E. The Applicant argues that the limitations as argued in examiner's labelled arguments A-D have not been met for claim 1 and therefore claims 2-4, and 7-8 are patentably distinct over Hajimiri et al. The evidence detailed in the arguments labelled A-D have proven that the rejection under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Application No.

2004/0222859 Hajimiri et al. over Claim 1 has been correctly anticipated, hence the rejections on claims 2-4, 7, and 8 are also anticipated by Hajimiri et al.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

An appeal conference was held on 11/28/06 with Mr. Victor A. Mandala Jr. (Patent Examiner), Mr. Ricky Mack, (Supervisory Patent Examiner), and Leonardo Andujar, (Acting Supervisory Examiner), as the conferees.

Respectfully submitted,

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